REMARKS

Claims 1-9, 11-15 and 17-23 are pending in this application. By this Amendment, the specification and claims 1-3, 8-9, 11-15, 17-18 and 21 are amended and claims 10 and 16 are cancelled without prejudice or disclaimer. Various amendments are made for clarity and are unrelated to issues of patentability.

The Office Action rejects claims 1-23 under 35 U.S.C. §102(e) by U.S. Patent Publication 2003/0056123 to Hseieh. The rejection is respectfully traversed with respect to the pending claims.

Independent claim 1 recites receiving a System Management Interrupt (SMI) signal, determining whether a bus master device is in an active state when the SMI signal is for performing CPU speed transition, and canceling the CPU speed transition operation when the bus master device is determined to be in the active state and generating a retry SMI signal at prescribed intervals.

Hseieh does not teach or suggest at least these features of independent claim 1. More specifically, the Office Action primarily cites Hseieh's paragraphs [0032]–[0035] for features of the claims including independent claim 1. Hseieh does not teach or suggest generating a retry SMI at prescribed intervals. Rather, Hseieh very clearly describes checking a peripheral busy counter to determine whether the counter is zero or not. Based on the counter, an isolation flag may be set or canceled and a frequency of a CPU can be adjusted. Hseieh does not teach or suggest cancelling a CPU speed transisition operation when the bus master device is determined

to be in the active state and generating a retry SMI signal at prescribed intervals as recited in independent claim 1.

Additionally, Hseieh does not teach or suggest receiving a System Management Interrupt (SMI) signal. Rather, Hseieh counts a number of times that an idle thread has been executed. This does not relate to receiving a system management interrupt (SMI) signal, as recited in independent claim 1.

For at least the reasons set forth above, Hseieh does not teach or suggest all the features of independent claim 1. Thus, independent claim 1 defines patentable subject matter.

Independent claim 8 recites interrupt occurrence reason recognition means for recognizing an occurrence reason of an interrupt signal, active state checking means for checking an active state of a predetermined device, and interrupt generating means for creating a second interrupt signal to retry the prescribed operation for the CPU speed transition when the interrupt occurrence reason recognition means determines that a first interrupt signal is for the CPU speed transition and the active state checking means determines that the predetermined device is in the active state, and the interrupt generating means creates the second interrupt signal based on a predetermined timer contained in the computer.

For at least similar reasons as set forth above, Hseieh does not teach or suggest all the features of independent claim 8. More specifically, Hseieh does not teach or suggest that the interrupt generating means creates the second interrupt signal based on a predetermined timer contained in the computer. In discussing previous dependent claim 10, the Office Action cites

Hseieh's paragraph [0034]. However, this paragraph at best merely describes a peripheral busy counter. This does not correspond to creating a second interrupt signal based on a predetermined timer. Accordingly, independent claim 8 defines patentable subject matter.

Independent claim 15 recites an interrupt generator coupled to the interrupt receiver and configured to generate a second interrupt signal to retry a prescribed operation needed for CPU speed transition when a first interrupt signal for the CPU speed transition is received and a bus master device is in an active state, and the interrupt generator generates the second interrupt signal based on a predetermined timer contained in the apparatus.

For at least similar reasons as set forth above, Hseieh does not teach or suggest at least these features of independent claim 15. More specifically, Hseieh does not teach or suggest the interrupt generator generates the second interrupt signal based on a predetermined timer. As discussed above, Hseieh's paragraph [0034] merely relates to a peripheral busy counter. This does not correspond to an interrupt signal based on a predetermined timer. Accordingly, independent claim 15 defines patentable subject matter.

Independent claim 21 recites an article including a machine-readable storage medium containing instructions that when executed, cause the computer system to receive an System Management Interrupt (SMI) signal, determine whether a bus master device is in an active state when the SMI signal is a first SMI CPU speed transition signal, and cancel the CPU speed transition operation when the bus master device is in the active state and generate an event at predetermined intervals.

For at least similar reasons as set forth above, Hseieh does not teach or suggest at least these features of independent claim 21. More specifically, Hseieh does not teach or suggest receiving an SMI signal. Still further, Hseieh does not teach or suggest to cancel the CPU's speed transition operation when the bus master device is in the active state and generate an event at predetermined intervals. Accordingly, independent claim 21 defines patentable subject matter.

For at least the reasons set forth above, each of independent claims 1, 8, 15 and 21 define patentable subject matter. Each of the dependent claims depends from one of the independent claims and therefore defines patentable subject matter at least for this reason. In addition, the dependent claims recite features that further and independently distinguish over the applied references.

For example, dependent claim 3 recites that the retry SMI signal generated at the prescribed intervals is one of a watchdog timer SMI signal and an embedded control SMI signal to retry the CPU speed transition operation. See also dependent claims 11 and 17. When discussing this feature, the Office Action appears to cite Hseieh's paragraph [0032], lines 4-13. However, the cited section does not relate to a watchdog timer SMI signal or an embedded control SMI signal. Accordingly, Hseieh does not teach or suggest the features of dependent claim 3. Thus, dependent claims 3, 11 and 17 (and corresponding dependent claims) define patentable subject matter at least for this additional reason.

Still further, dependent claim 9 recites the first interrupt signal for the CPU speed transition is responsive to a change of CPU use amount, switching between AC adapter and

battery power sources, reduction of battery lifetime, runtime setup of a user and temperature variation. When discussing this claim, the Office Action cites Hseieh's paragraph [0032], lines 4-13. However, these features merely relate to counting a number of times that an idle thread has been executed and comparing that number with the default number of times. This does not teach or suggest the features of dependent claim 9. Thus, dependent claim 9 defines patentable subject matter at least for this additional reason.

Still further, dependent claim 12 recites that the second interrupt signal is created at intervals of a predetermined time determined by a system BIOS. The Office Action cites Hseieh's paragraph [0032], lines 4-6 for these features. However, the cited section does not relate to creating a second interrupt signal at intervals of a predetermined time. Accordingly, dependent claim 12 defines patentable subject at least for this additional reason.

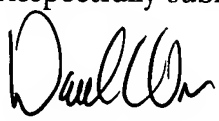
CONCLUSION

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-9, 11-15 and 17-23 are earnestly solicited. If the Examiner believes that any additional changes would place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this,

concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,



David C. Oren
Registration No. 38,694

P.O. Box 221200
Chantilly, Virginia 20153-1200
(703) 766-3777 DCO/kah

Date: May 17, 2007

Please direct all correspondence to Customer Number 34610